ABSTRACT OF THE DISCLOSURE

Disclosed is a manufacturing method capable of easily manufacturing a semiconductor device exhibiting a high reliability but no decrease in a field isolation voltage due to an influence by overetching. Field oxide is formed on a silicon substrate by a LOCOS method. Polysilicon is deposited on the surface of the field oxide and on the surface of a silicon nitride layer formed on the silicon substrate when forming the field oxide layer. The polysilicon layer is deposited thicker than a thickness of the silicon nitride layer. The polysilicon layer deposited on the silicon nitride layer and on the field oxide is removed by polishing like a CMP method, whereby the surface of the silicon nitride layer is exposed. A structure having the polysilicon layer existing on only the surface of the field oxide is obtained by removing the silicon nitride layer. The polysilicon layer functions as a protective layer for the field oxide, thereby preventing the field oxide layer 34 from being etched when in overetching.